

ELEC3730 Embedded Systems Lecture 8: The Intel Architecture Processor

- History
- Real vs Protected Mode introduction
- Registers
- Segmented Memory Architecture



The Intel Processor Family

Name	Date	Transistors	Microns	Clock speed	Data width	MIPS
8080	1974	6,000	6	2 MHz	8 bits	0.64
8088	1979	29,000	3	5 MHz	16 bits 8-bit bus	0.33
80286	1982	134,000	1.5	6 MHz	16 bits	1
80386	1985	275,000	1.5	16 MHz	32 bits	5
80486	1989	1,200,000	1	25 MHz	32 bits	20
Pentium	1993	3,100,000	0.8	60 MHz	32 bits 64-bit bus	100
Pentium II	1997	7,500,000	0.35	233 MHz	32 bits 64-bit bus	~300
Pentium III	1999	9,500,000	0.25	450 MHz	32 bits 64-bit bus	~510
Pentium 4	2000	42,000,000	0.18	1.5 GHz	32 bits 64-bit bus	~1,700
Pentium 4 "Prescott"	2004	125,000,000	0.09	3.6 GHz	32 bits 64-bit bus	~7,000

8086 Microprocessor

Common Signals		
Name	Function	Type
AD16-AD0	Address/Data Bus	Bidirectional
A16-AD0	Address/Status	Output
AD16-AD0	Bus High Enable	Output
MEM/IO	Memory/Maximum Mode Control	Input
RD	Read Control	Output
TEST	Wayside Test Control	Input
READY	Wait State Control	Input
RESET	System Reset	Input
NMI	Non-Maskable Interrupt	Input
INTR	Interrupt Request	Input
CLK	System Clock	Input
VCC	Supply	Input
GND	Ground	Input
Minimum Mode Signals (MN/MX = V _{CC})		
Name	Function	Type
RDY	Ready Signal	Input
HLDA	Hold Acknowledge	Output
TR	Tristate Control	Output
M/IO	Memory/IO Control	Output
DT/R	Data Transfer/Receive	Output
DR	Data Enable	Output
A16-AD0	Address/Status	Output
INTA	Interrupt Acknowledge	Output
Maximum Mode Signals (MN/MX = GND)		
Name	Function	Type
RDY _{1,2}	Ready Signal/Status	Bidirectional
LD/CS	Bus Priority Lock	Output
RDY ₃	Bus Cycle Status	Output
CS1-CS0	Interrupt Control	Output

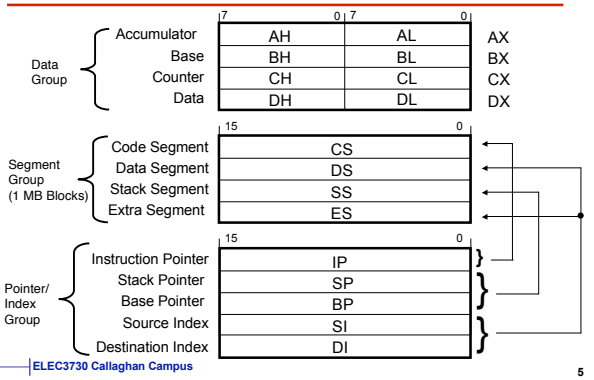


Figure 4-1. 8086 Pin Definitions

Operating Modes of Intel Architecture (IA) Processors

- **Real-address Mode:**
 - Corresponds to the original 8086 processor;
 - Supported by all processors in the IA family;
 - Initial operating mode when a hardware reset signal applied (eg. start-up);
 - Limited number of processor features are available in real mode;
 - Physical address space is limited to one megabyte.
- **Protected Mode:**
 - Originally introduced with the Intel 286;
 - Enhanced in the Intel 386.
 - Offers greater performance than real mode;
 - All processor features available;
 - Larger physical address space available.
- **System Management Mode**
 - Not considered here

8086/8088 Registers = IA Real Mode Registers

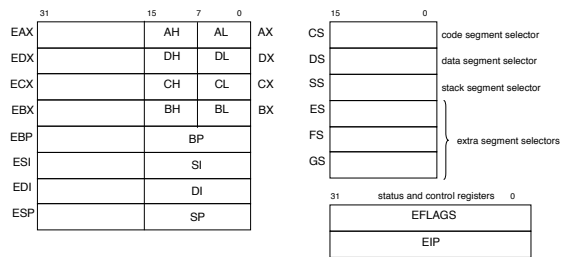


AX, BX, CX, DX - Some Specialized Uses

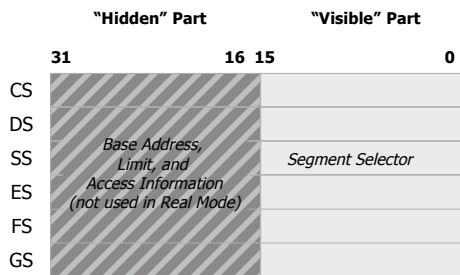
Accumulator	7	0	7	0	
Base	AH		AL		AX
Counter	BH		BL		BX
Data	CH		CL		CX
	DH		DL		DX

- AX, Accumulator
 - Main Register for Performing Arithmetic
 - mult/div must use AH, AL
 - "accumulator" Means Register with Simple ALU
- BX, Base
 - Point to Translation Table in Memory
 - Holds Memory Offsets; Function Calls
- CX, Counter
 - Index Counter for Loop Control
- DX, Data
 - After Integer Division Execution - Holds Remainder

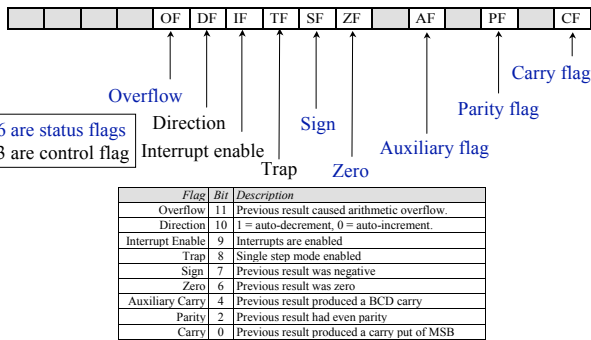
IA Protected Mode Registers



Segment Registers



Flags Register



Segmented Memory Architecture

- One program can work on several sets of data;
- Only logical addresses need be specified – can be relocated to many different physical addresses.
- Extra hardware and software complexity;
- One segment (8086) = 2^{16} = 64KB – software limited to segment size
- 80386 – protected mode introduced to remove above limitation.

